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DATE: Monday, June 28, 2004

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		DB=USPT,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR	
☐	L28	l9.clm. and l19	7
☐	L27	l9.ab. and l19	1
☐	L26	l9 and l19	41
☐	L25	l10 and l19	0
☐	L24	l4 and l19	9
☐	L23	l3.clm. and L19	71
☐	L22	l2.clm. and L19	327
☐	L21	l2.ab. and L19	165
☐	L20	l2 and L19	820
☐	L19	l12 or l13 or l14 or l15 or l16 or l17 or L18	1790
☐	L18	710/300.ccls.	246
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☐	L16	710/33.ccls.	446
☐	L15	710/20.ccls.	319
☐	L14	710/13.ccls.	123
☐	L13	710/3.ccls.	311
☐	L12	710/2.ccls.	293
☐	L11	L10 same (control$4 adj (input or signal$4))	15
☐	L10	l2 same L9	180
☐	L9	(read adj access) same (write adj access)	2659
☐	L8	L6 same (data near2 input) same (data near2 output)	2
☐	L7	L6 same (data adj input) same (data adj output)	0
☐	L6	l5 same (control$4 near2 (input or signal$4))	24
☐	L5	(access$4 near2 (type or kind)) near5 ((storage or memory) adj device)	507
☐	L4	(access$4 near2 (type or kind)) with ((storage or memory) adj device)	687
☐	L3	access$4 near3 ((storage or memory) adj device)	26062
☐	L2	((storage or memory) adj device)	289494
☐	L1	6557047.pn. or 6138173.pn. or 6735638.pn.	5

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L24: Entry 9 of 9 File: USPT Feb 9, 1982

DOCUMENT-IDENTIFIER: US 4315308 A

**** See image for Certificate of Correction ****

TITLE: Interface between a microprocessor chip and peripheral subsystems

Brief Summary Text (11):

Briefly, the present invention utilizes a single bidirectional address/control/data bus in combination with two simplex control lines to perform all complex address control and data transfer functions. This is accomplished by assigning different functions to these lines during sequential cycles of a data transfer operation. During a first cycle the bus carries a control data specification and the low order bits of the peripheral address. The control specification is encoded to provide information indicating the type of access (memory device or I/O device), the direction of data transfer (read or write), the length of data to be transferred (1 byte, 2 bytes, etc.), and modifier bits which further define the type of access being undertaken. Interprocessor communication (IPC) is signaled during this first cycle by lowering the simplex control line from the peripheral device to the microprocessor.

Current US Original Classification (1):

710/33

L11: Entry 10 of 15 File: USPT Jul 16, 1996

DOCUMENT-IDENTIFIER: US 5537660 A
**** See image for Certificate of Correction ****
TITLE: Microcontroller having selectable bus timing modes based on primary and secondary clocks for controlling the exchange of data with memory

Brief Summary Text (5):
Semiconductor microcontroller chips generally incorporate a certain amount of program and/or data memory on-chip. For various reasons such as prototyping, large memory requirements, program updates, etc., microcontrollers also need to access external memory devices. Such access is usually done over a multiplexed address/data system bus under the control of a few dedicated control signals carrying information such as when the address is valid, whether the access is a read or a write access, and whether a read access is for code or data.

L11: Entry 11 of 15 File: USPT Jun 11, 1996

DOCUMENT-IDENTIFIER: US 5526320 A
TITLE: Burst EDO memory device

CLAIMS:

15. A memory device having a plurality of data nodes for receiving and driving a plurality of data signals, an array of memory elements, and a plurality of address nodes for receiving a row and a column address, the memory device comprising:

a row address strobe node for receiving a row address strobe signal for latching the row address in the memory device;

a write control signal node for receiving a write control signal for selecting between read and write accesses of the memory device; and

first and second column address strobe nodes for receiving first and second column address strobe signals, wherein either of said first and second column address strobe signals latch the column address, and either of said first and second column address strobe signals being active during a read access of the memory device will enable data to be driven on each of the data nodes, and only a first plurality of the data signals will be stored in the array in response to said write control signal selecting a write access and said first column address strobe node being active and said second column address strobe node being inactive.

L11: Entry 6 of 15 File: USPT Jul 22, 1997

DOCUMENT-IDENTIFIER: US 5651138 A
TITLE: Data processor with controlled burst memory accesses and method therefor

Brief Summary Text (10):
In computer systems, a central processing unit (CPU) accesses memory by providing an address which indicates a unique location of a group of memory cells which collectively store the accessed data element. The CPU initiates what is referred to as a bus cycle by providing the address to an address bus, and one or more control signals to signal that the address is valid and the bus cycle has begun. A read/write control signal then indicates whether the access is to be a read access or a write access. Subsequently, a data element is either read from a data bus if the bus cycle is a read cycle, or provided to the data bus if the bus cycle is a write cycle. A memory device to accommodate such accesses is connected to the address and data buses, and provides data to the data bus during a read cycle, or stores data on the data bus during a write cycle, at a location indicated by the address on the address bus. This type of bus cycle requires at least two clock cycles, and typically may require four or more clock cycles.

L11: Entry 5 of 15 File: USPT Feb 10, 1998

DOCUMENT-IDENTIFIER: US 5717654 A
TITLE: Burst EDO memory device with maximized write cycle timing

Detailed Description Text (20):
The operation of the circuit of FIG. 3 is further described in the timing diagram of FIG. 4. Signals are labeled according to the signal lines on which they are generated from the circuit of FIG. 3. Circuit initialization will occur at the beginning of each access cycle in response to an access cycle strobe signal active edge. In one embodiment of the circuit of FIG. 3, the access cycle strobe signal is a column address strobe (/CAS) for a burst mode DRAM as described in the present invention, and a new cycle begins with each falling edge of /CAS in a burst access. After initialization, a write cycle operation will begin in response to the latched read/write control signal. The write operation will continue until the end of the access cycle (the beginning of a subsequent access). Once the next cycle is begun, a new column will be selected as fast as possible. Rapid termination of the write cycle is important to prevent data at the next column address from being disturbed. By selecting the access cycle strobe signal, the write operation may be rapidly terminated at the beginning of the next cycle without waiting for the command latch to be cleared. The timing diagram of FIG. 4 shows a read cycle followed by three write cycles and then another read cycle. A read access begins at time t1. Signal 56 being high in this embodiment signifies a read access. Once the access cycle strobe signal 50 transitions high, a read state on the read/write command signal is latched in the command latch which generates the latched read/write control signal. The transition to a write command on the read/write command signal line 56 is ignored until time t2. At time t2 a write cycle begins. After the signal pulse on line 54, a write state of the read/write command is latched on signal line 60 until it is cleared by the next signal pulse on line 54 at time t3. For each write cycle, the latched read/write control signal passes through the multiplexer to line 68. The select line 64 switches during each write cycle after the access cycle strobe signal has transitioned high, causing the multiplexer to select the access cycle strobe signal. At the beginning of the next cycle, the access cycle strobe signal transitions low terminating the write, clearing the command latch and resetting the select signal. For burst write access cycles, the write control signal on line 68 is active for a period of time approaching an access cycle time despite the operating frequency of the memory device. The write control signal is only cleared between burst write cycles for a period of time required to select a new column of the memory array. At time t5, a read cycle begins. The command latch and select line are cleared, and the select line remains low for the read cycle.

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L8: Entry 2 of 2 File: USPT Apr 9, 1974

DOCUMENT-IDENTIFIER: US 3803363 A
TITLE: APPARATUS FOR THE MODIFICATION OF THE TIME DURATION OF WAVEFORMS

Brief Summary Text (11):
In a specific embodiment, analog input data in the form of speech is sampled at a continuously variable first rate and each sample is converted to a digital word representation and applied to a random access memory type of storage device for storage under the control of an input pointer (e.g., address register) access control that is incremented at the first rate. An output pointer (e.g., address register) access control, incremented at the second rate, controls the transmission of digital word representations from the storage device to a digital to analog decoder for conversion into analog form. In time compression, the series of input digital words are monitored for positive to negative zero crossing characteristics, while in time expansion, a search for the same characteristic in the output digital words is made in a lead or look ahead offset relation to the output pointer. An indication of each such detected characteristic is saved. An indication of a particular one of such detected characteristics is also saved and when a predetermined relation between input and output access controls is reached on detection of a saved indication in the output data, that segment is terminated and a new segment initiated with the location of the saved particular one. Such retention may be achieved in a variety of ways including storage of a marker in memory with the data having the detected characteristic. In the specific embodiment, a corresponding digital word and an incremented value of the memory address of that digital word are saved. Each such data replaces prior saved data so that the particular saved value is the most recent detected value.

L6: Entry 1 of 24 File: USPT May 20, 2003

DOCUMENT-IDENTIFIER: US 6567904 B1
TITLE: Method and apparatus for automatically detecting whether a memory unit location is unpopulated or populated with synchronous or asynchronous memory devices

Detailed Description Text (24):
The memory unit type detection:and control logic 108 of one embodiment includes an asynchronous DRAM (ADRAM) state machine 205 and an SDRAM state machine 209 to control the respective memory access control signals. The required memory access control signals depend, not only on the type of memory device being accessed, but also on the state that the memory device is in. Such state machines are described in detail in a copending patent application assigned to Intel Corporation, the assignee of the invention, entitled "Memory Controller for Independently Supporting Synchronous and Asynchronous DRAM Memories," Ser. No. 08/767,853, filed Dec. 17, 1996, now U.S. Pat. No. 5,721,860, which is continuation of Ser. No. 08/248,301, filed May 24, 1994, now abandoned. The memory device states and state transitions for both asynchronous DRAM devices and SDRAM devices are well-known to those of ordinary skill in the art, and described in data sheets available from the individual DRAM manufacturers. The asynchronous DRAM state machine 205 and the SDRAM state machine 209 operate in conjunction with the configuration registers 201, the address-to-memory unit decoder 207 and the signal select mux 217 to provide memory access control signals to meet the memory access protocol requirements, including timing requirements of the particular types of memory devices in each of the memory unit locations 221-224. The term protocol is used herein to refer to both the types and timing of particular signals used when accessing a particular type of memory device.

L6: Entry 2 of 24 File: USPT May 15, 2001

DOCUMENT-IDENTIFIER: US 6233179 B1
TITLE: Circuit and method for reading and writing data in a memory device

Brief Summary Text (14):
In another embodiment, the present invention provides a memory device. The memory device includes an array of addressable memory cells that are coupled to digit and word lines. An address circuit selects a cell in the array. The memory device also includes a sense amplifier that is coupled to control the voltage on a pair of digit lines for the selected cell of the memory device. The memory device includes input/output transistors that couple the pair of digit lines to a pair of input/output lines. A control circuit of the memory device determines the type of access to be executed for the selected cell of the memory device and generates a variable voltage control signal to activate the input/output transistors of the memory array based on the type of access so as to couple data between the digit lines and the input/output lines.

L6: Entry 8 of 24 File: USPT Jun 18, 1996

DOCUMENT-IDENTIFIER: US 5528552 A
TITLE: Dynamic random access memory device with sense amplifiers serving as cache memory independent of row address buffer unit for high-speed sequential access

Detailed Description Text (65):
Although particular embodiments of the present invention have been shown and described, it will be obvious to those skilled in the art that various changes and modifications may be made without departing from the spirit and scope of the present invention. For example, a dynamic random access memory device according to the present invention may have more than four memory cell arrays, and the present invention is applicable to a static type random access memory device having sense amplifiers respectively associated with digit line pairs. Moreover, the dynamic random access memory device according to the present invention may be split into more than one part respectively fabricated on semiconductor chips, and may form a part of a large scale integration together with other function blocks. Finally, the row address strobe signal RAS, the restore control signal RSTR and the row and column address signals may be produced by logic circuits integrated on a semiconductor chip together with the dynamic random access memory device according to the present invention.

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L6: Entry 12 of 24 File: USPT Feb 22, 1994

DOCUMENT-IDENTIFIER: US 5289570 A
TITLE: Picture image editing system for forming boundaries in picture image data in a page memory device

Detailed Description Text (58):
An Image Bus Arbiter 125, arbitrates the various kinds of accesses to the page memory device 102 in accordance with the predetermined order of priority. When a request signal is input from either the input side DMA control circuit 122 or from the output side DMA control circuit 124, Image Bus Arbiter 125 accepts either one of the requests on the basis of the priority just mentioned. Then, the Image Bus Arbiter 125 causes whichever one of the input side DMA control circuit 122 and the output side DMA control circuit 124 corresponds to the accepted request signal to generate a prescribed control signal.